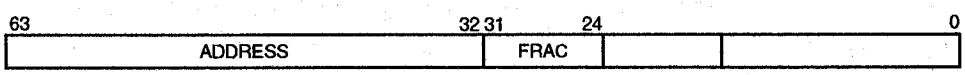
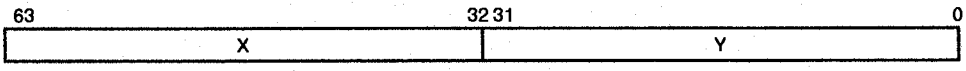
Blitter Registers

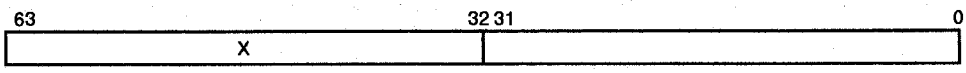
BLT_ADDR_0,1,2



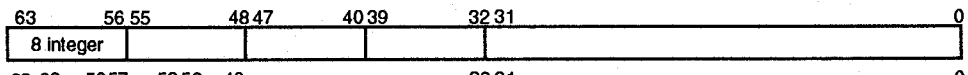
BLT_CLIP_s
BLT_CLIP_BR
BLT_CLIP_UL
BLT_START_XY

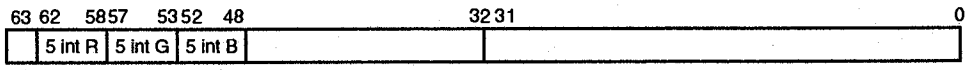


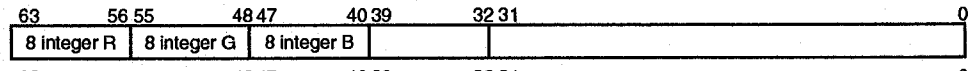
BLT_CLIP_DELTA_X

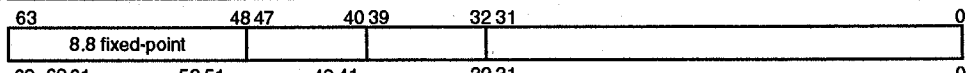


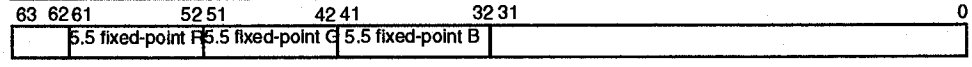
BLT_COLOR_0,1,V_DELT

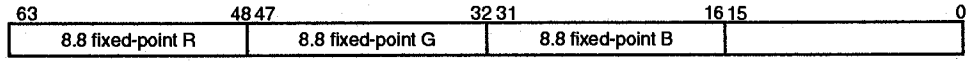




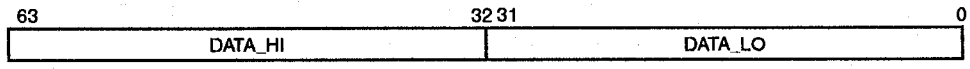




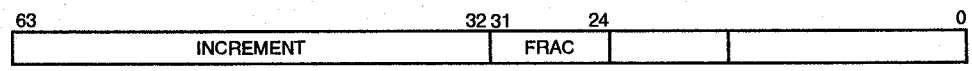




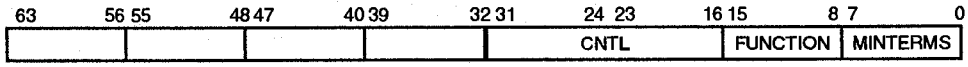
BLT_DATA



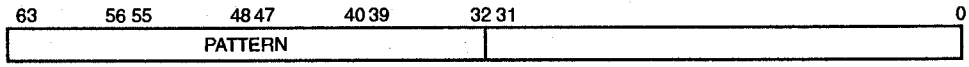
BLT_DELTA_s
BLT_DELTA_X_0,1,2
BLT_DELTA_Y_0,1,2
BLT_DELTA_DELTA_X,Y
BLT_DELTA_X,Y_LINE



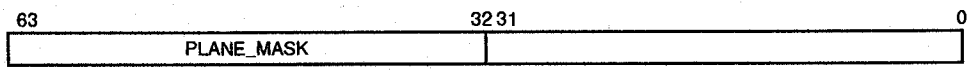
BLT_FUNC



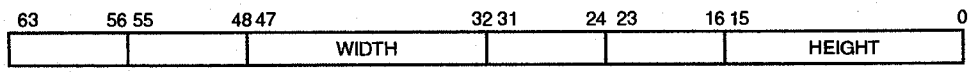
BLT_PATTERN_32



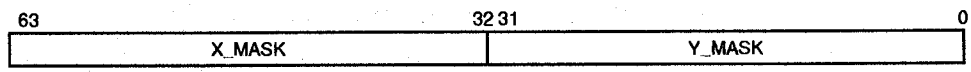
BLT_PLANE_MASK



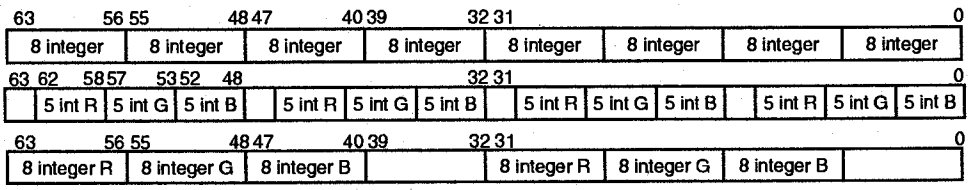
BLT_SIZE



BLT_TEX_ADDR_CNTL



BLT_TRANS_COLOR



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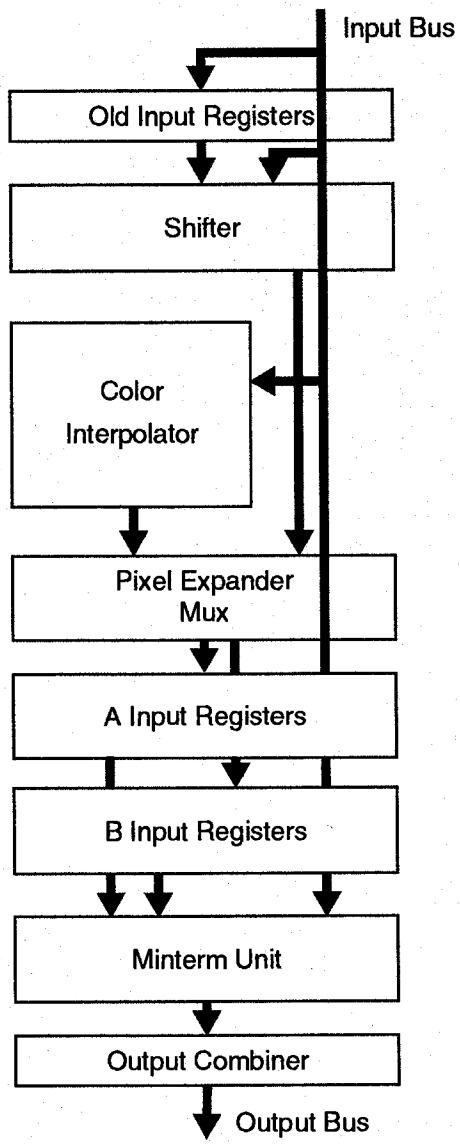
Blitter Datapath



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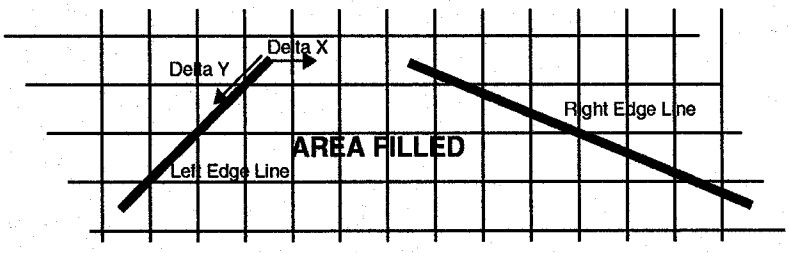
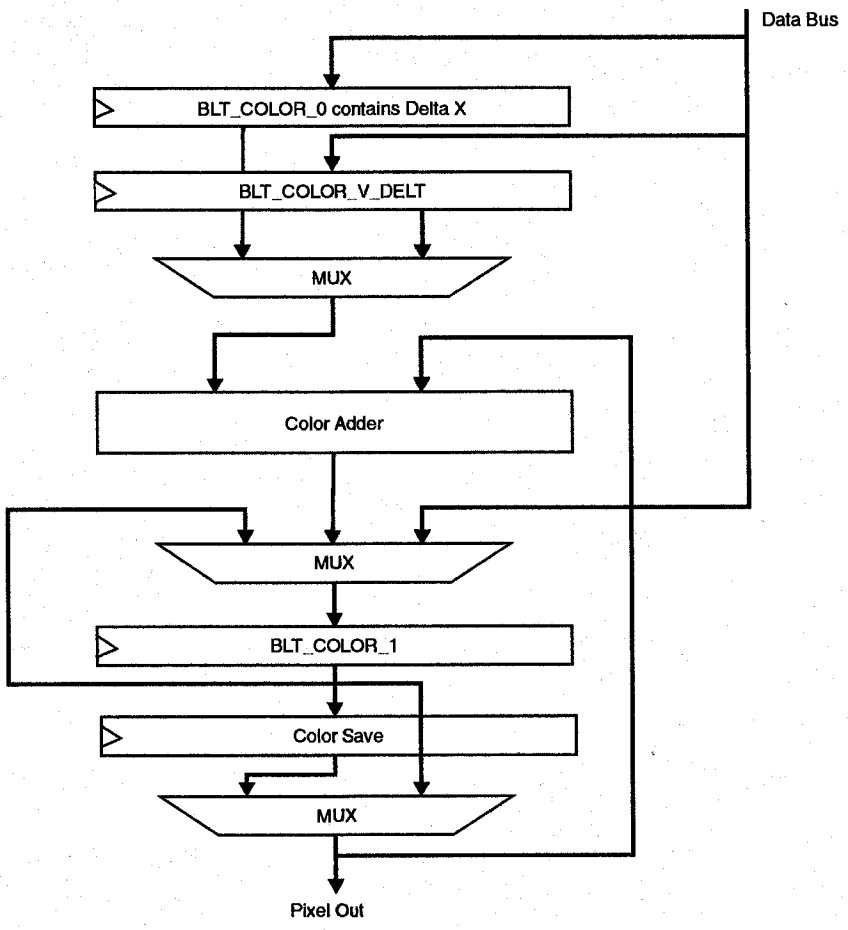
Blitter Assisted Shading and Texture Mapping



Color Interpolator



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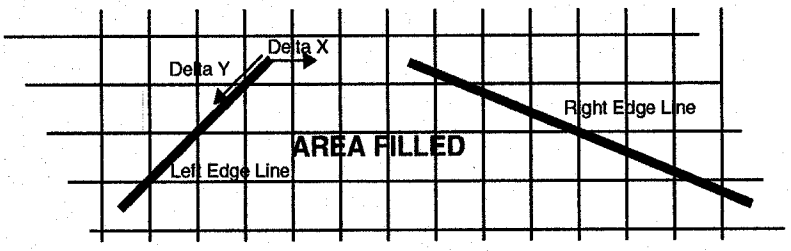
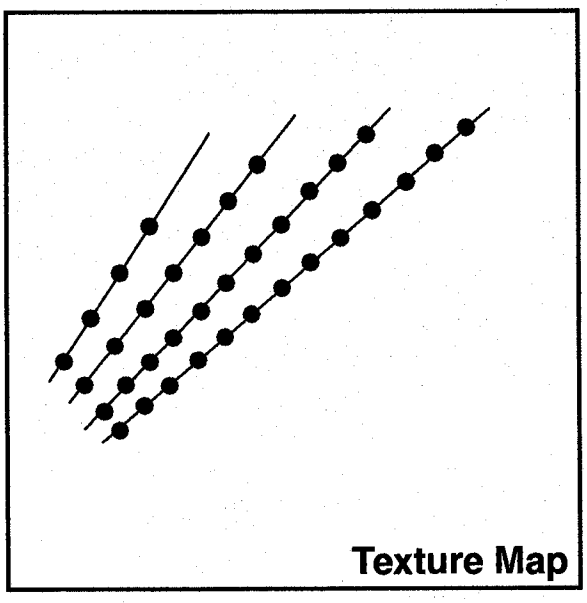
Textured Fills





- **Each pixel is individually fetched from texture map**
- **Texture map addressing uses fixed-point arithmetic**
- **Delta x,y and start position updated after each scan line**

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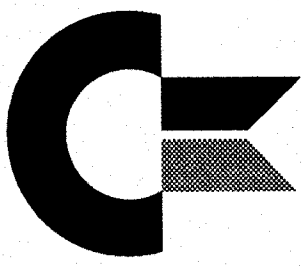

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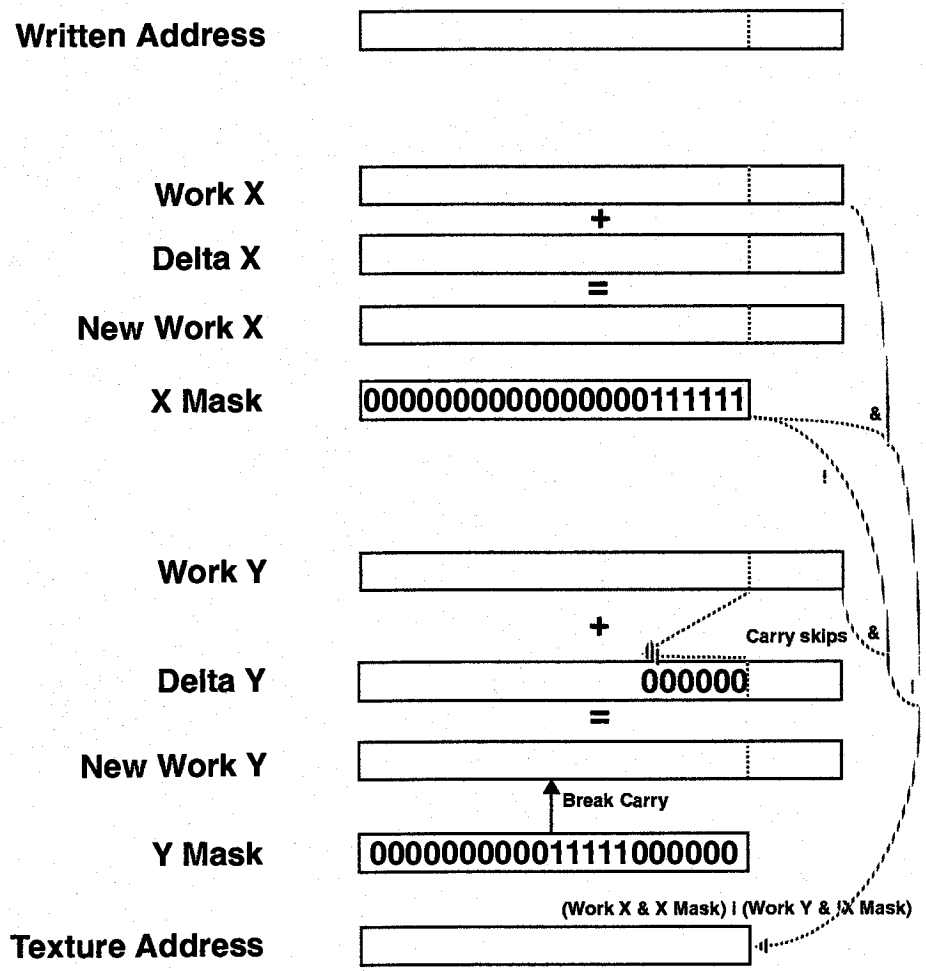
Texture Address Generation



- **@ Start**
  - Save X <- Written Addr
  - Save Y <- Written Addr
  - Goto Setup
- **@ Setup**
  - Work X <- Save X
  - Work Y <- Save Y
- **@ Each Pixel**
  - Texture Addr <- (Work X & X Mask) | (Work Y & !X Mask)
  - Work X <- Work X + Delta X
  - Work Y <- Work Y + Delta Y
- **@ Line End**
  - Delta X <- Delta X + Delta Delta X
  - Delta Y <- Delta Y + Delta Delta Y
  - Save X <- Save X + Delta X Line
  - Save Y <- Save Y + Delta Y Line
  - Goto Setup

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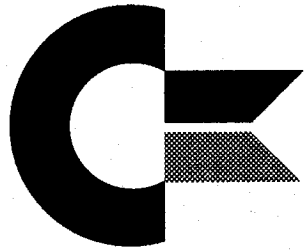

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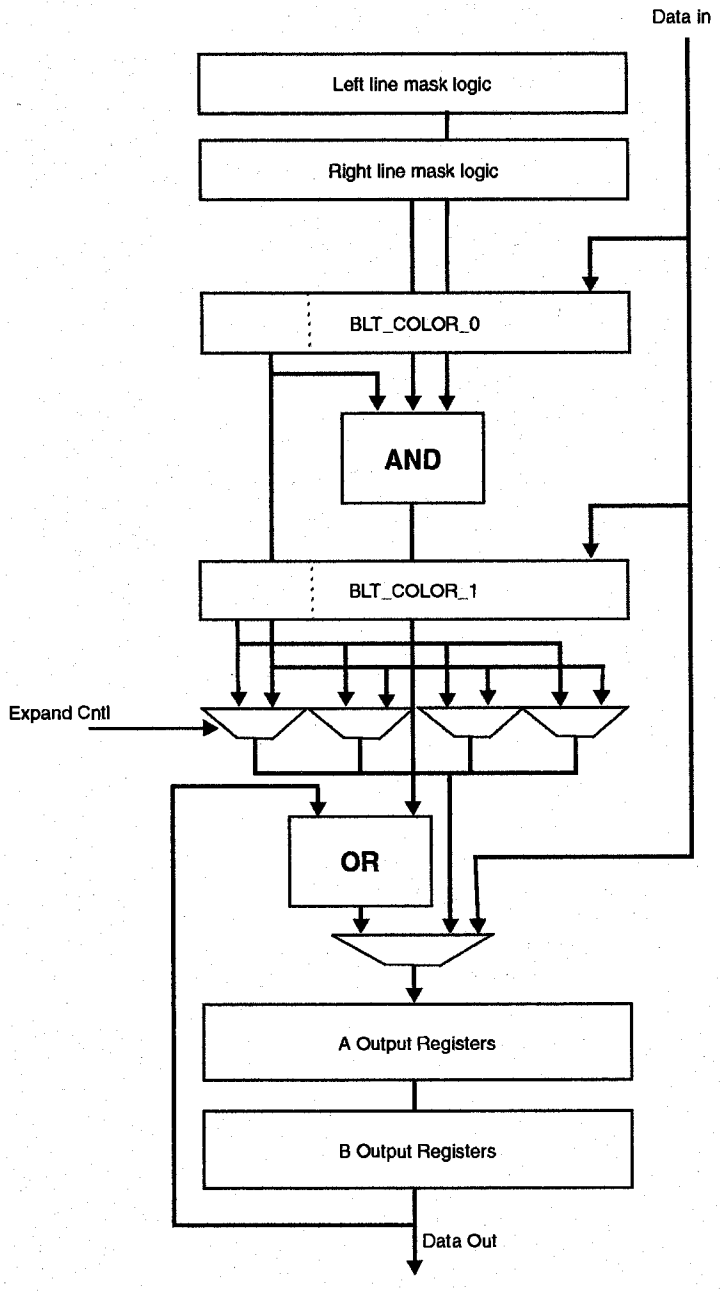
Blitter Assisted Line Drawing and Pixel Expansion



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Peripheral Bus Interface (PBI)

- **Byte Interface for Hombre Chip Set**
  - Supports up to four peripheral chips (4 channels)
  - Each channel has its own register address space
  - 6 address lines (from address bits 8:3)
  - Programmed I/O from internal RISC Processor
  - DMA to/from Display memory, System memory , PCI
  - Common Interrupt line
- **Round-Robin priority scheme for DMA**
- **Programmed I/O has priority over DMA**
- **DMA must be occur to/from double-word aligned locations**

- **Configuration Register per channel:**
  - Intel / Motorola Protocol
  - Cycle length
    - Use positive wait
    - Use negative wait
    - 1 cycle wait
    - 3 cycle wait
  - DMA direction
    - Memory to peripheral
    - Peripheral to memory
  - DMA transfer size
    - 8, 16, 32 bytes
  - DMA Acknowledge Protocol
    - Normal cycle with dack
    - Transfer on dack
  - Address to chip-select delay
    - 1, 2 cycles
  - Chip-select to data-strobe delay
    - 0, 1 cycles

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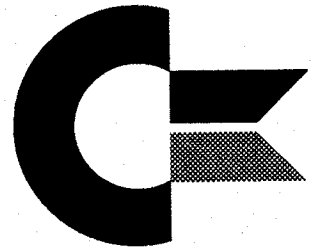

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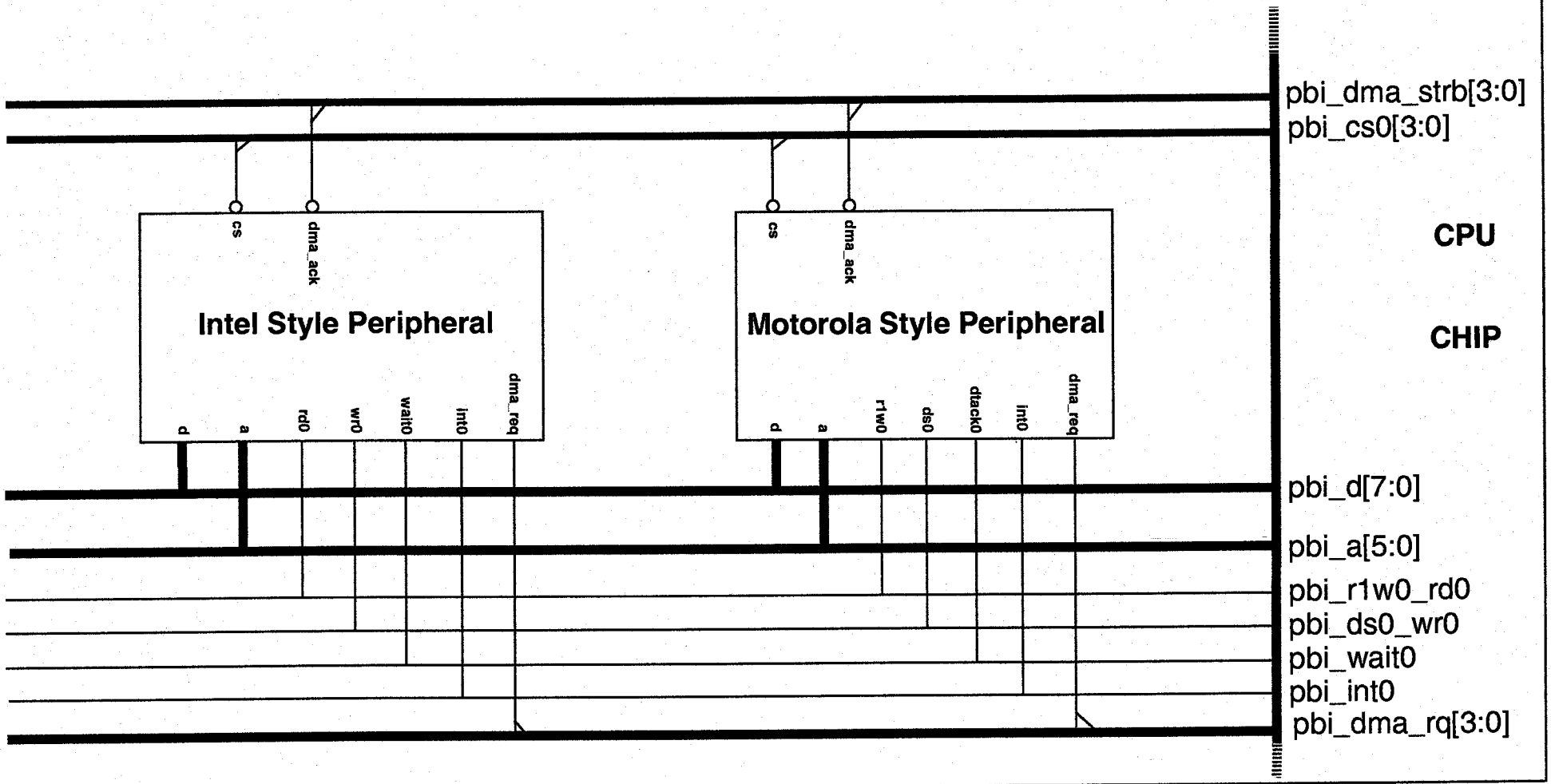
PBI Provides Glue-Free Interface to Byte Peripherals



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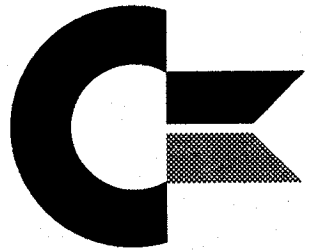

Commodore Confidential

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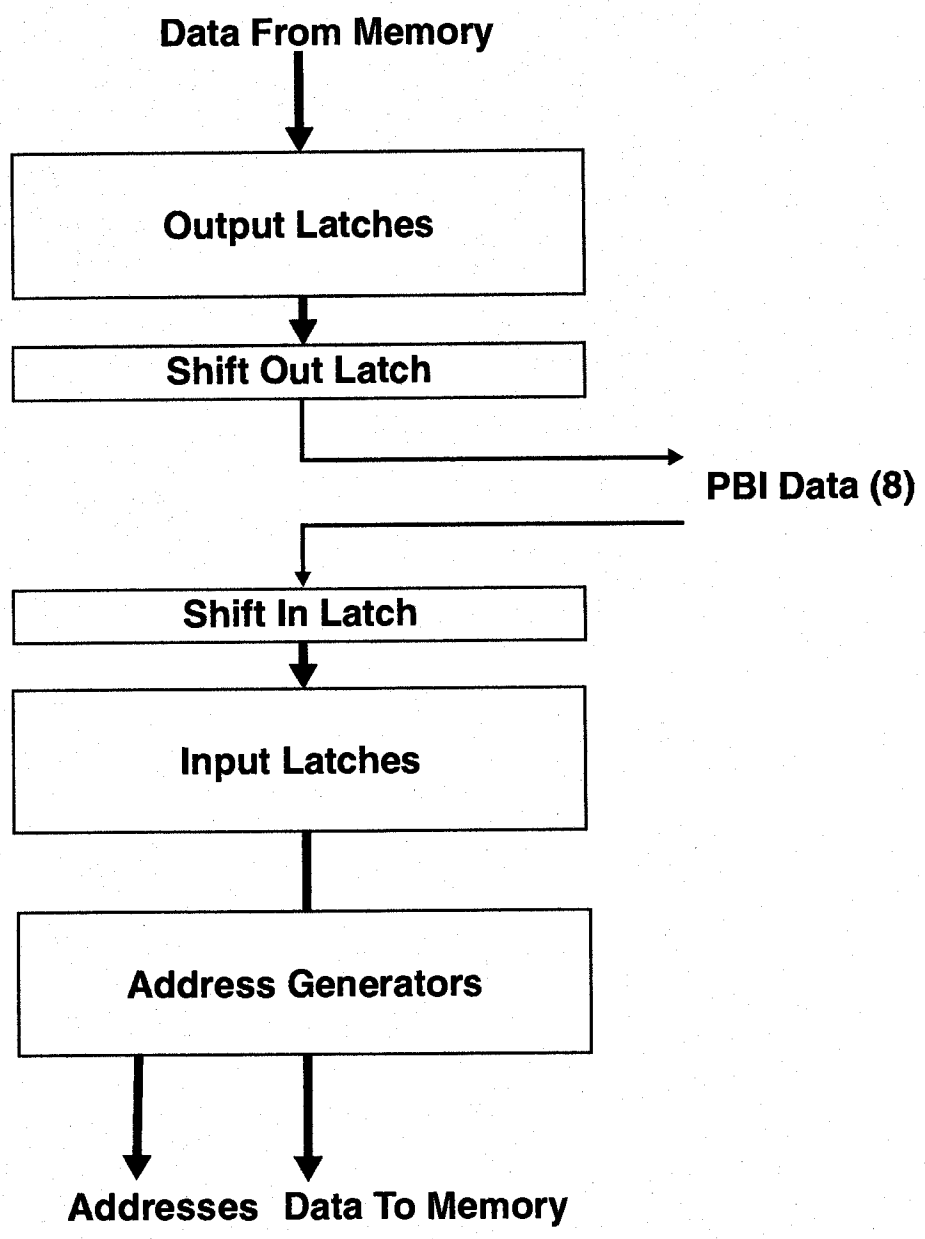
PBI Datapath



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Copper

- Video Line Synchronized "RISC" co-processor
- Executes lists of simple instructions including:
  - MOVE: Load an HOMBRE register with a value
  - JUMP: Execute from a new list address
  - WAIT: Wait for a specified video line or relative video line
- One level of hardware supported subroutine provided
- Interrupted each vertical blank event
- No "position enable" bits as in Amiga
- No horizontal matching as in Amiga
- JUMP instructions contain their target versus Amiga jumps which required writing a COP(1/2)(L/H) register

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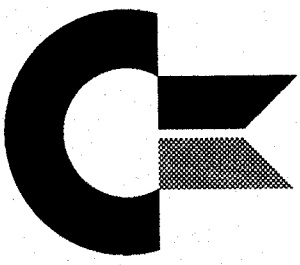

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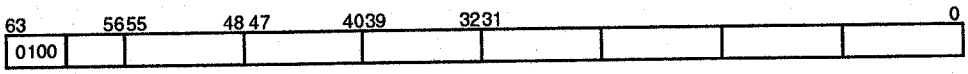
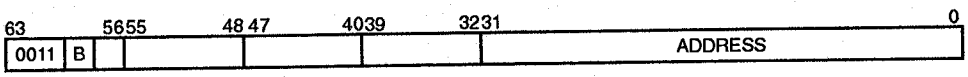
Copper Instructions

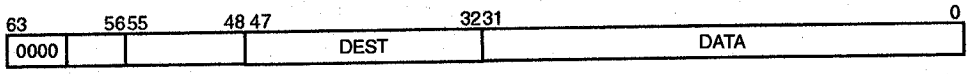
Clear Relative



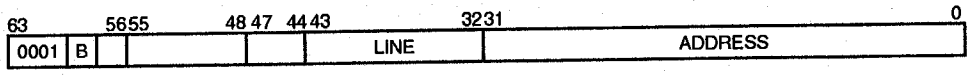
Jump



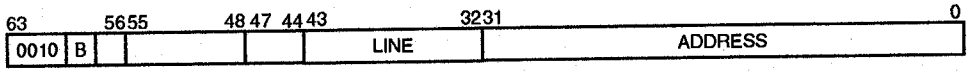
Move



Wait

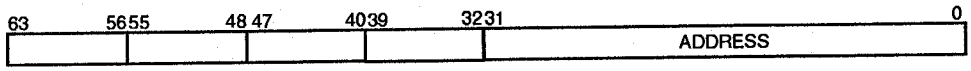


Wait Relative



Copper Register

COPR_VB_ADDR



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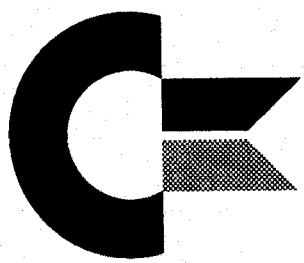

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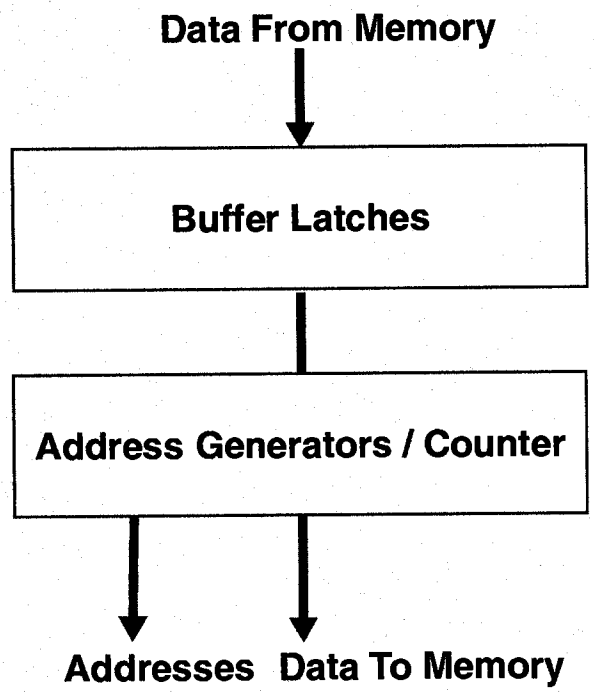
System Copier

- **Memory to Memory Copy / Fill**
- **Copies *n* 64-bit doublewords from source to destination**
- **Fills *n* 64-bit doublewords from CPU written latch to destination**
- **Useful for data block copy, memory initialization**
- **Consider it an "Independent, Simple minded blitter channel"**
- **Utilizes burst mode memory accesses**
  - **64-bit memory: ~ 65 Mbyte/sec moves - ~ 130 Mbyte/sec fills**
  - **32-bit memory: ~ 40 Mbyte/sec moves - ~ 80 Mbyte/sec fills**



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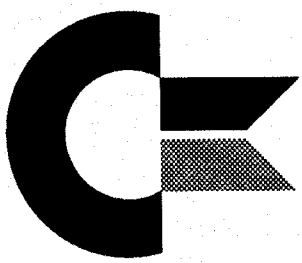

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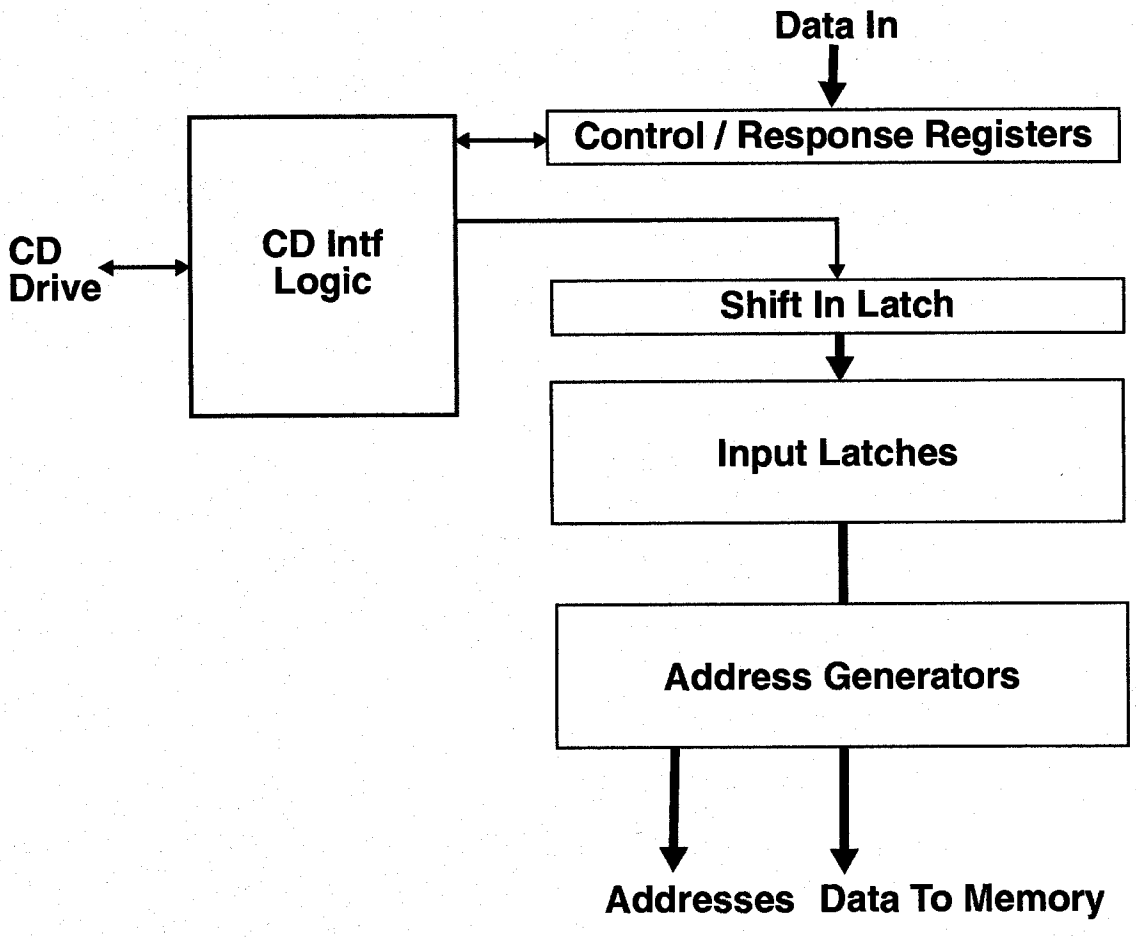
CD-ROM Interface

- Similar functionality as in "Akiko" of CD^{32}
- Utilizes burst mode memory accesses
- Easily capable of 2X or greater speed.
- 3 wire data interface from drive
- Serial control/response interface to/from drive
- Data Integrity is a combination of hardware and software



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Audio

- 12 AAA style, 16-bit, 44.1 Khz, CD quality channels
  - Will have 8-bit mode
  - ADPCM ??
- 2 CD formatted serial input lines
  - Each has L + R... results in total of 16 source channels
  - 3 wire (Data, Bclk, Lrck) input
  - One input (L + R) can be sampled into memory
- 1 CD formatted (L + R) serial output line
  - Intended to go to external postprocessor/amplifier
- Postprocessor / Amplifier
  - External
  - Provides tone / volume control for headphone line
  - Provides line-out for connection to stereo, etc.
  - Controlled via I^2C Bus

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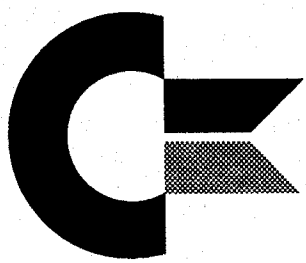

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Display/System Memory Controllers

- **Configurable for 9, 10, or 11 bit multiplexed memory addresses**
- **120 ns memory cycle**
  - **One word read: 120 ns**
  - **Four word burst: 240 ns**
- **Configurable for memory organizations:**
  - **32 bit (80 Mbytes/sec - 200 Mbytes/sec graphics)**
  - **64 bit (133 Mbytes/sec - 400 Mbytes/sec graphics)**
- **Burst across page boundary**
- **Supports RMW cycles for individual byte writes**
- **RAS decoding for 4 banks**
- **VRAM access control**
- **CAS before RAS refresh**

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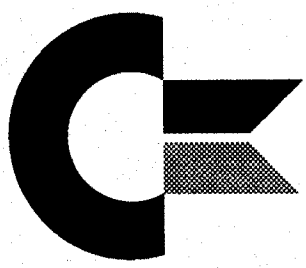

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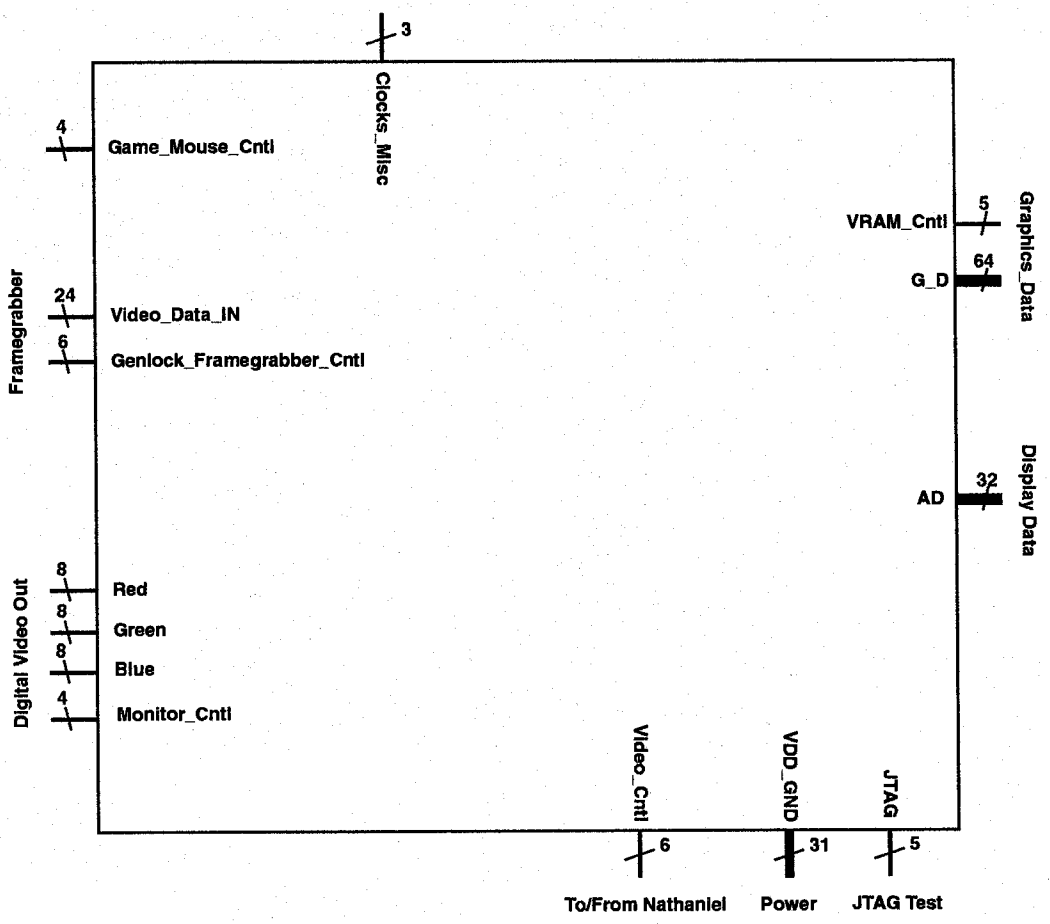
Video Chip (Natalie)



- **Functions:**
  - Line Buffers
  - Cursor Ram
  - 512 x 25 CLUT
  - Framegrabber
  - Genlock
  - YUV -> RGB (MPEG)
  - Mouse/Game Cntrlr Intf
- **Interfaces:**
  - 32/64-bit Graphics Data (VRAM)
  - 32-bit Display Memory (high 32)
  - 24-bit Digital RGB out (ext D/A)
  - 24-bit (option to 8+16) Video IN
  - Serial Mouse - Game Control
- **177 Signals / 31 Power-Ground**
  - 208 PQFP (225 BGA)

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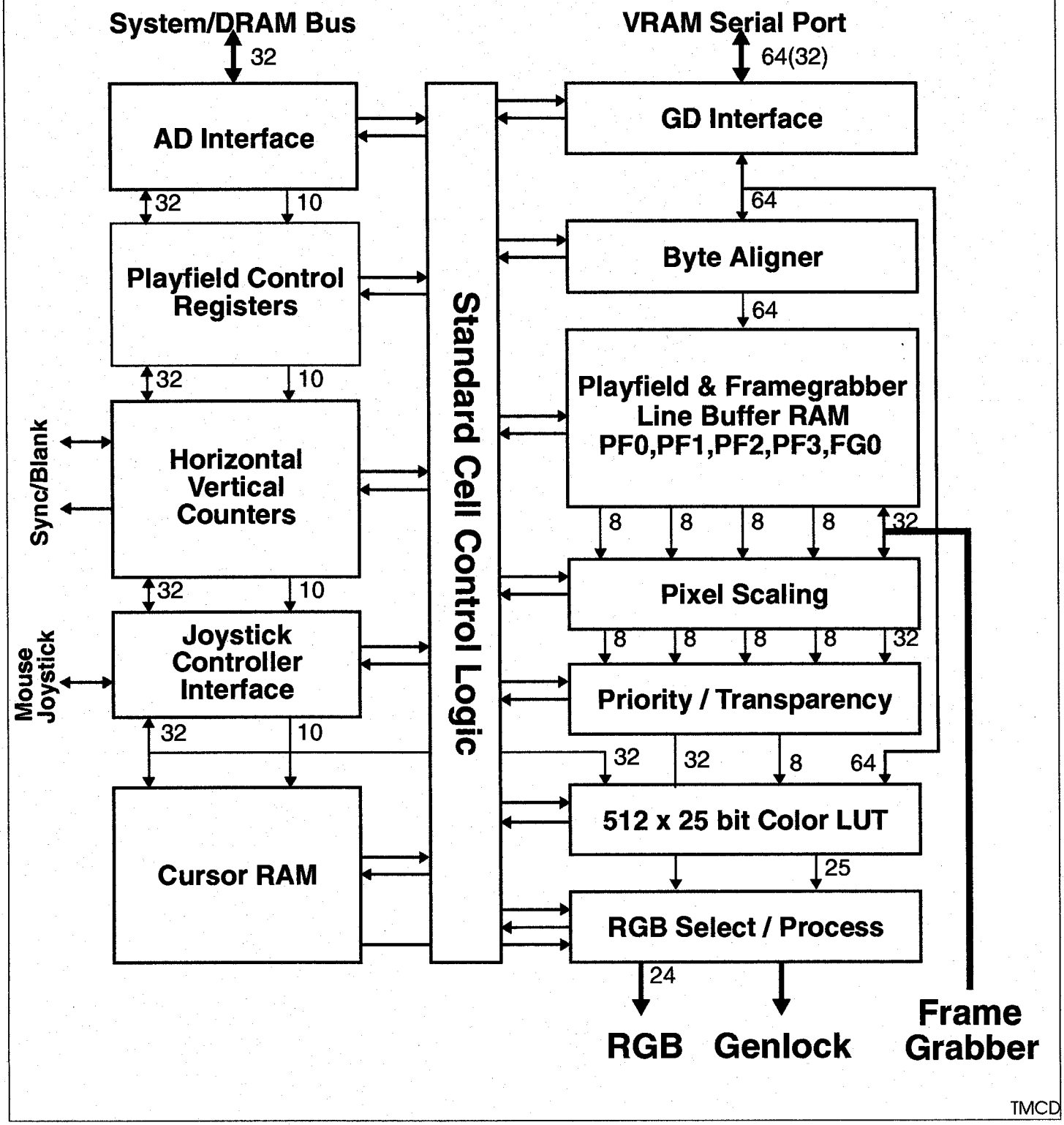
Functional Block Diagram of Video Chip



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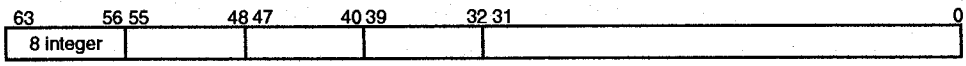
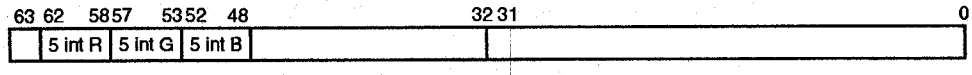
Video Modes

Pixel Formats

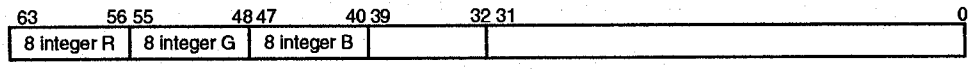
- **8-bit palette, HAM8:**



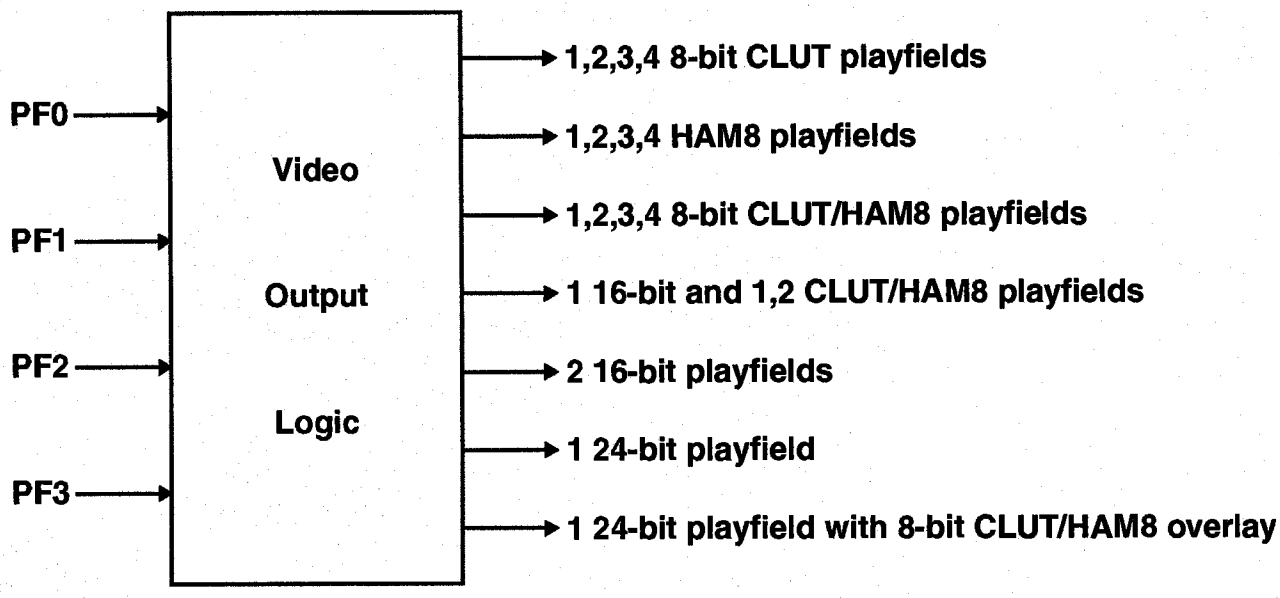
- **16-bit RGB (Hi-color):**



- **24(32)-bit RGB (True-color):**



Output Selection



Each playfield is individually positionable, scrollable, and scalable

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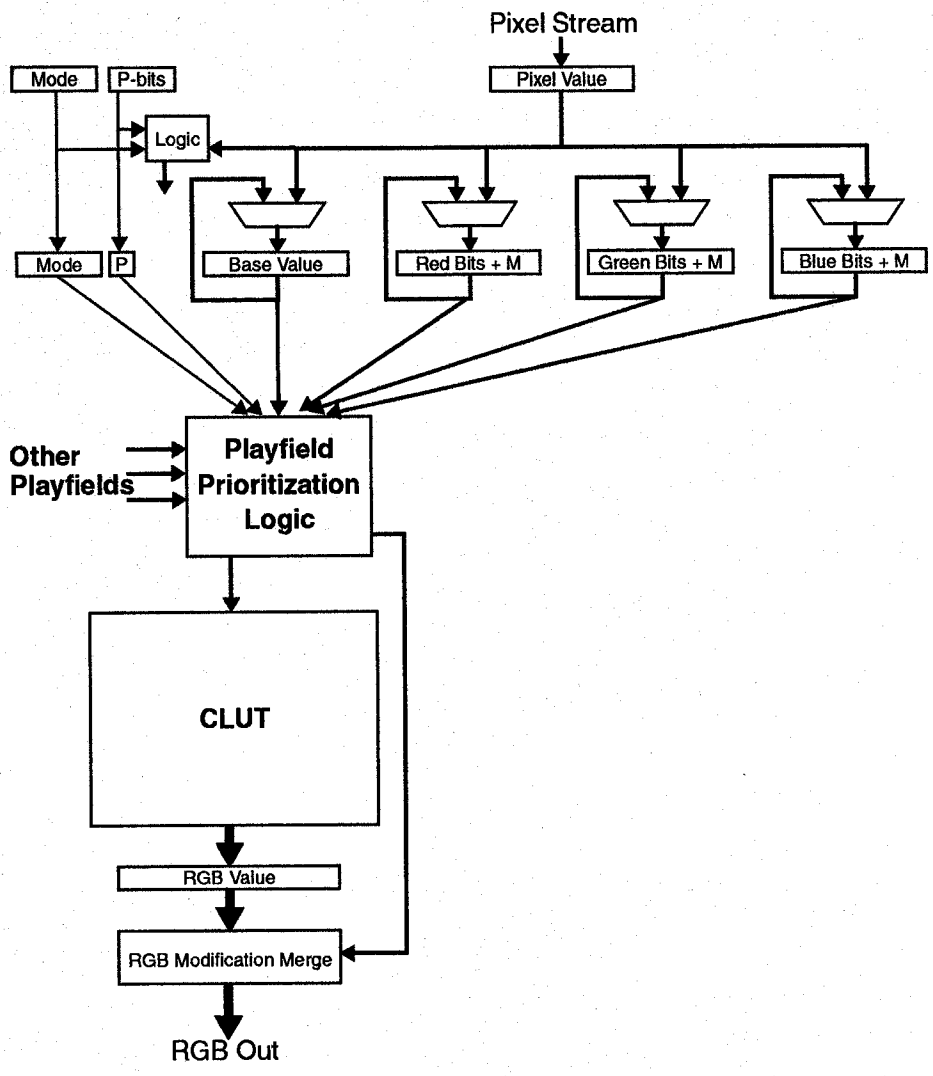
HAM8 Video Mode Operation



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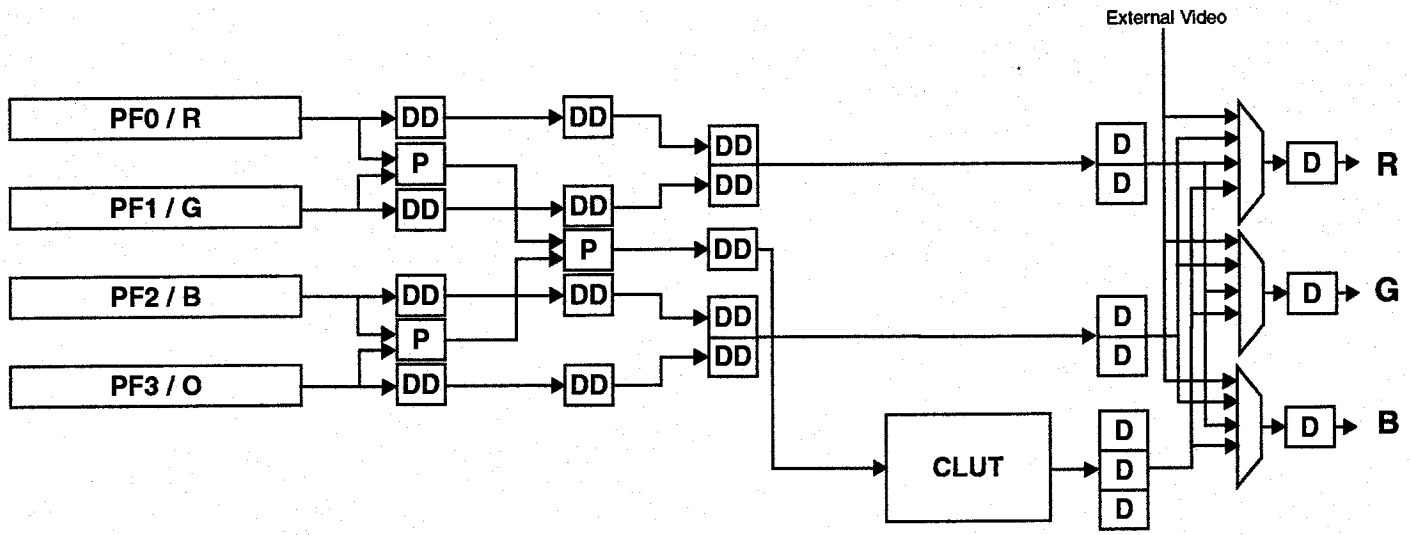
Video Output Processing



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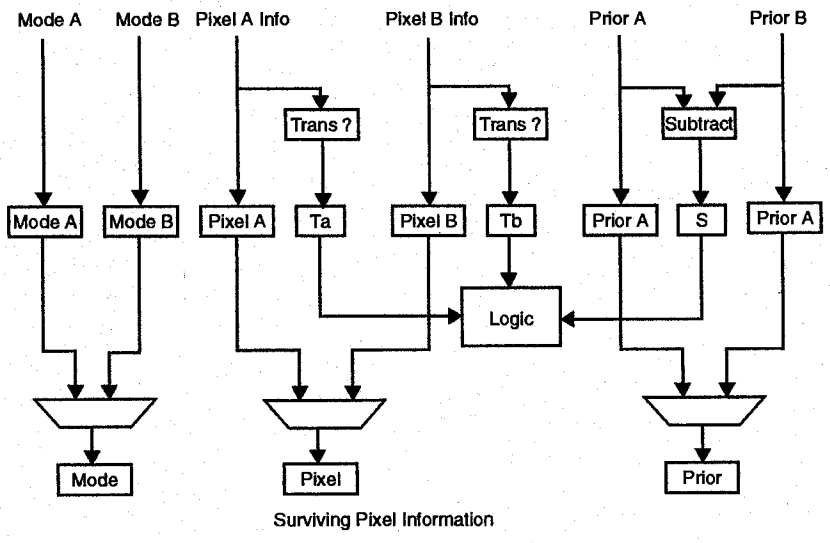
Pixel Prioritization



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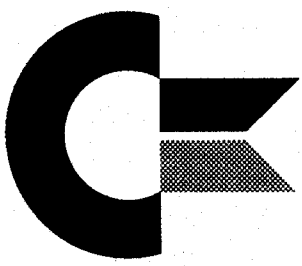

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Playfield Scaling

- **Playfields are independently scaleable both vertically and horizontally.**
- **The scaling ranges from 1/2 to 16x in increments of 1/16**
- **The entire playfield image is loaded into the line buffer each line**
- **Fractional scaling is achieved by either skipping or repeating the n-th pixel or line as it is being read from the line buffer.**

Scale factor:
x-scale 0x1.0 (1)
y-scale 0x1.0 (1)

1	2	3	4	5	6	7	8
9	A	B	C	D	E	F	0
8	7	6	5	4	3	2	1
0	F	E	D	C	B	A	9

Scale factor:
x-scale 0x1.8 (1-1/4)
y-scale 0x1.4 (1-1/2)

1	2	3	4	4	5	6	7	8	8
9	A	B	C	C	D	E	F	0	0
9	A	B	C	C	D	E	F	0	0
8	7	6	5	5	4	3	2	1	1
0	F	E	D	D	C	B	A	9	9
0	F	E	D	D	C	B	A	9	9

Scale factor:
x-scale 0x0.8 (1/2)
y-scale 0x0.8 (1/2)

1	3	5	7
8	6	4	2

Scale factor:
x-scale 0x2.2 (2-1/8)
y-scale 0x0.C (3/4)

1	1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	8
9	9	A	A	B	B	C	C	D	D	E	E	F	F	0	0	0
8	8	7	7	6	6	5	5	4	4	3	3	2	2	1	1	1

TMCD

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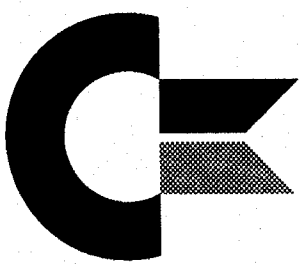

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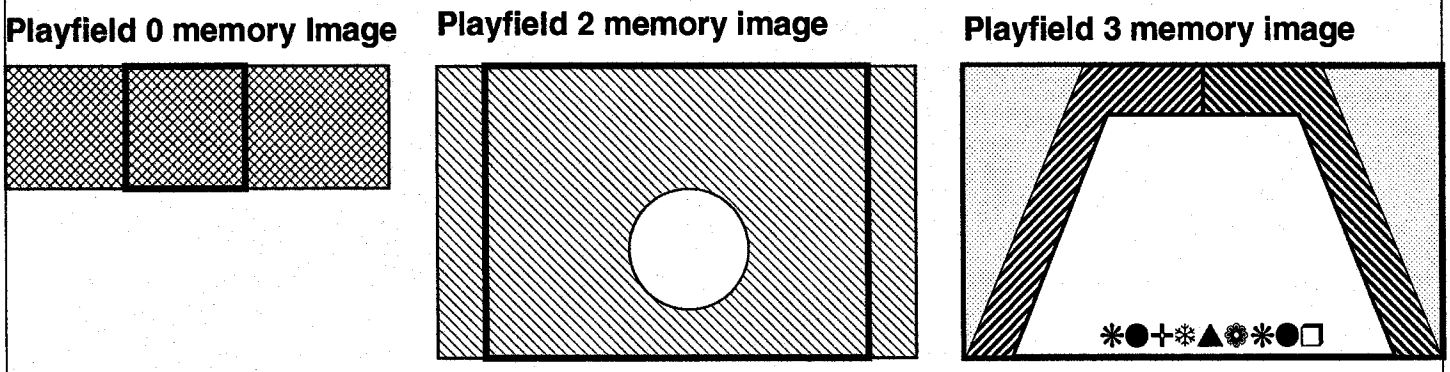
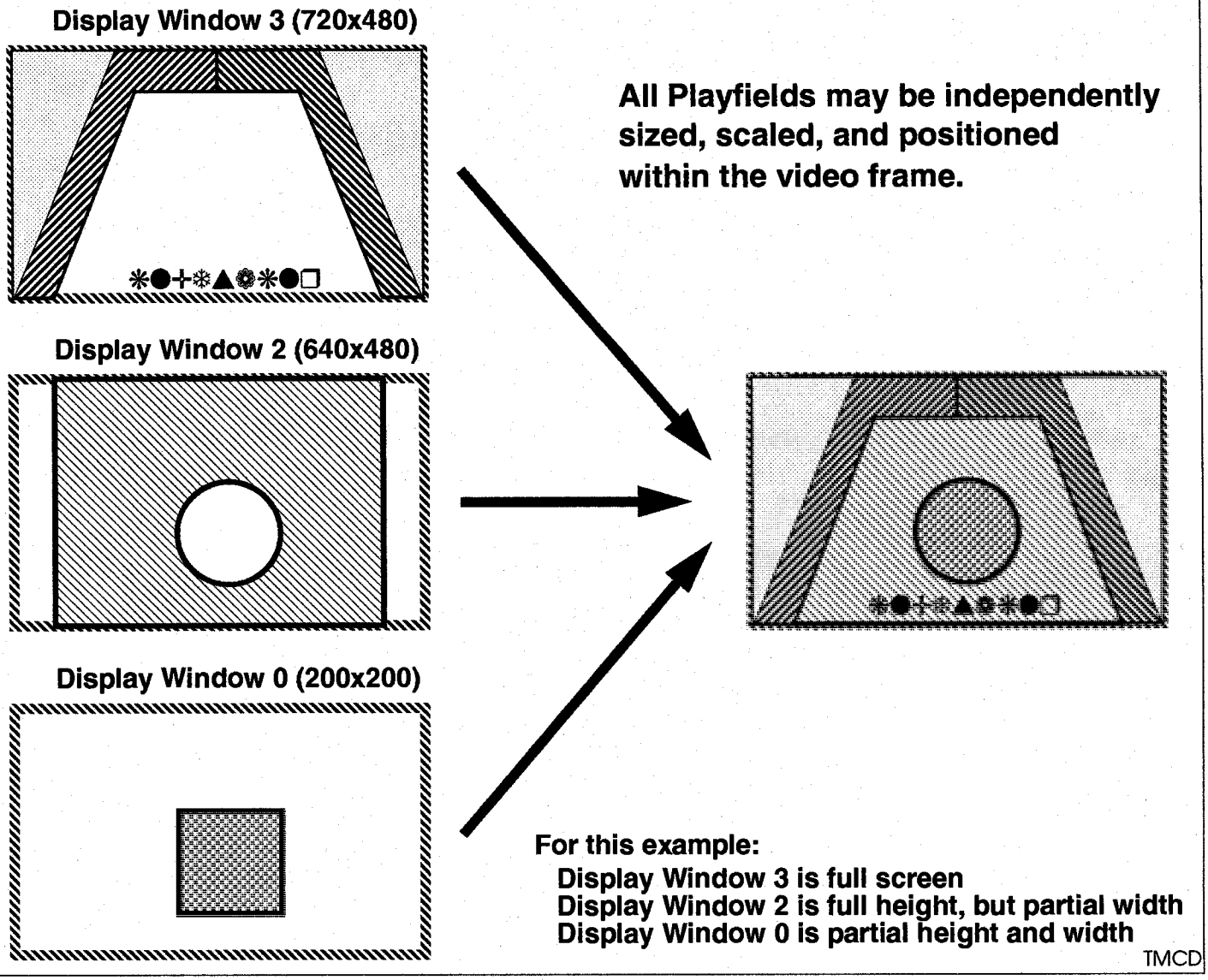
Playfield Display Windows





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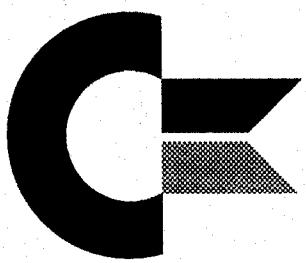

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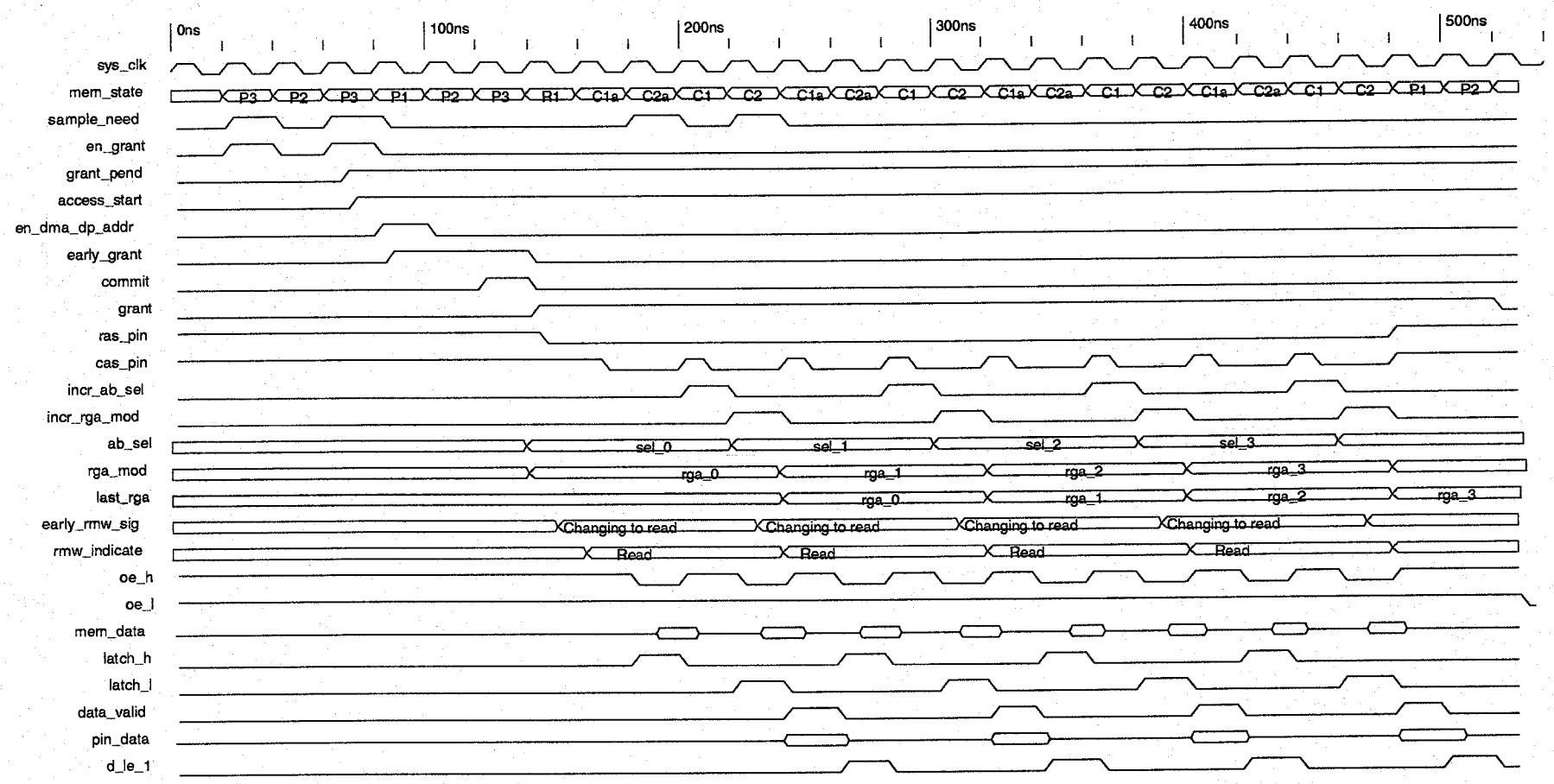
32 bit Memory Read Access



Read Non-Interleaved
32-bit Bus
64-bit Access
"read_32.td"

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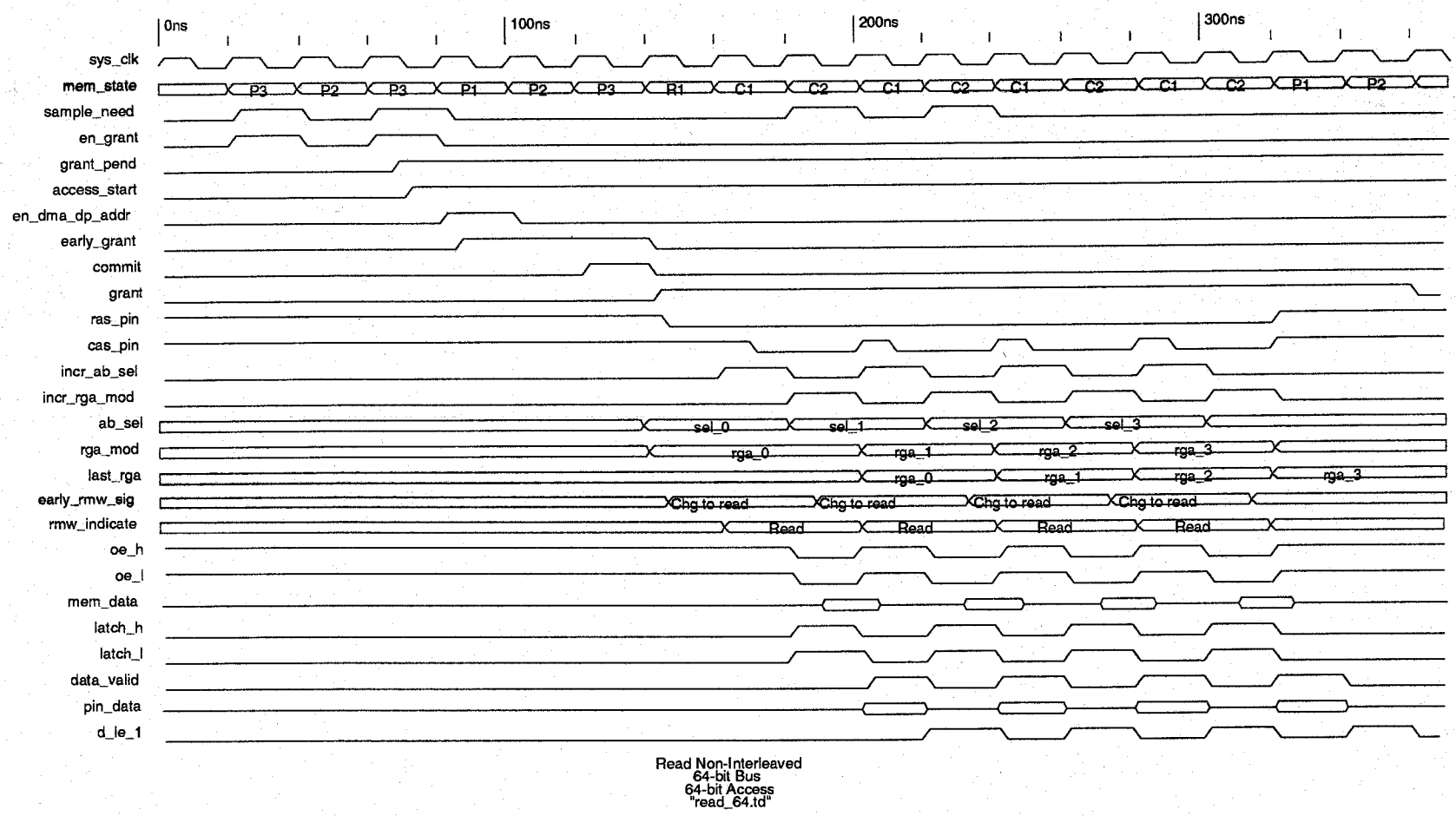
64-bit Memory Read Access



Read Non-Interleaved
64-bit Bus
64-bit Access
"read_64.td"

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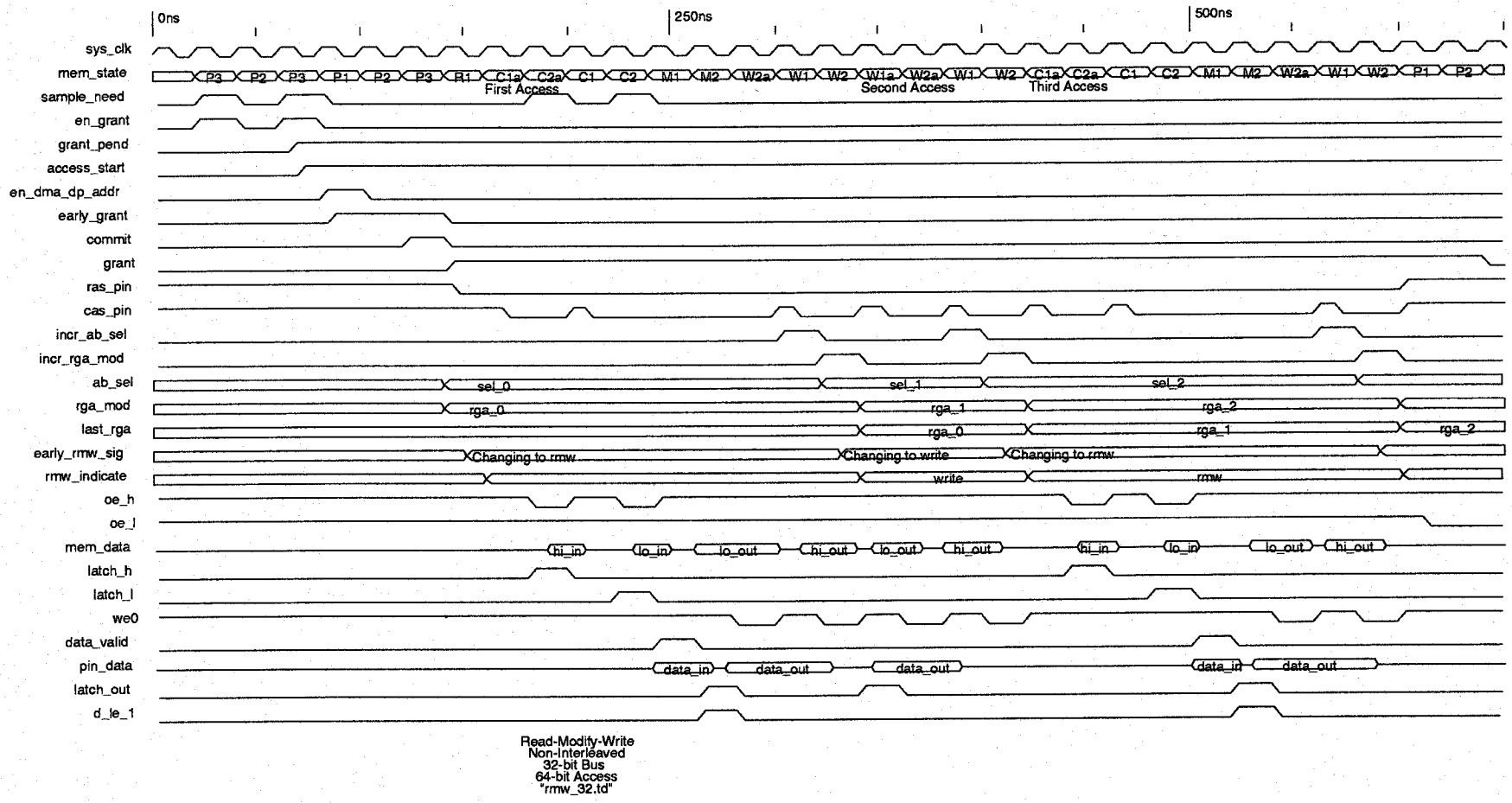
32-bit Memory RMW Access



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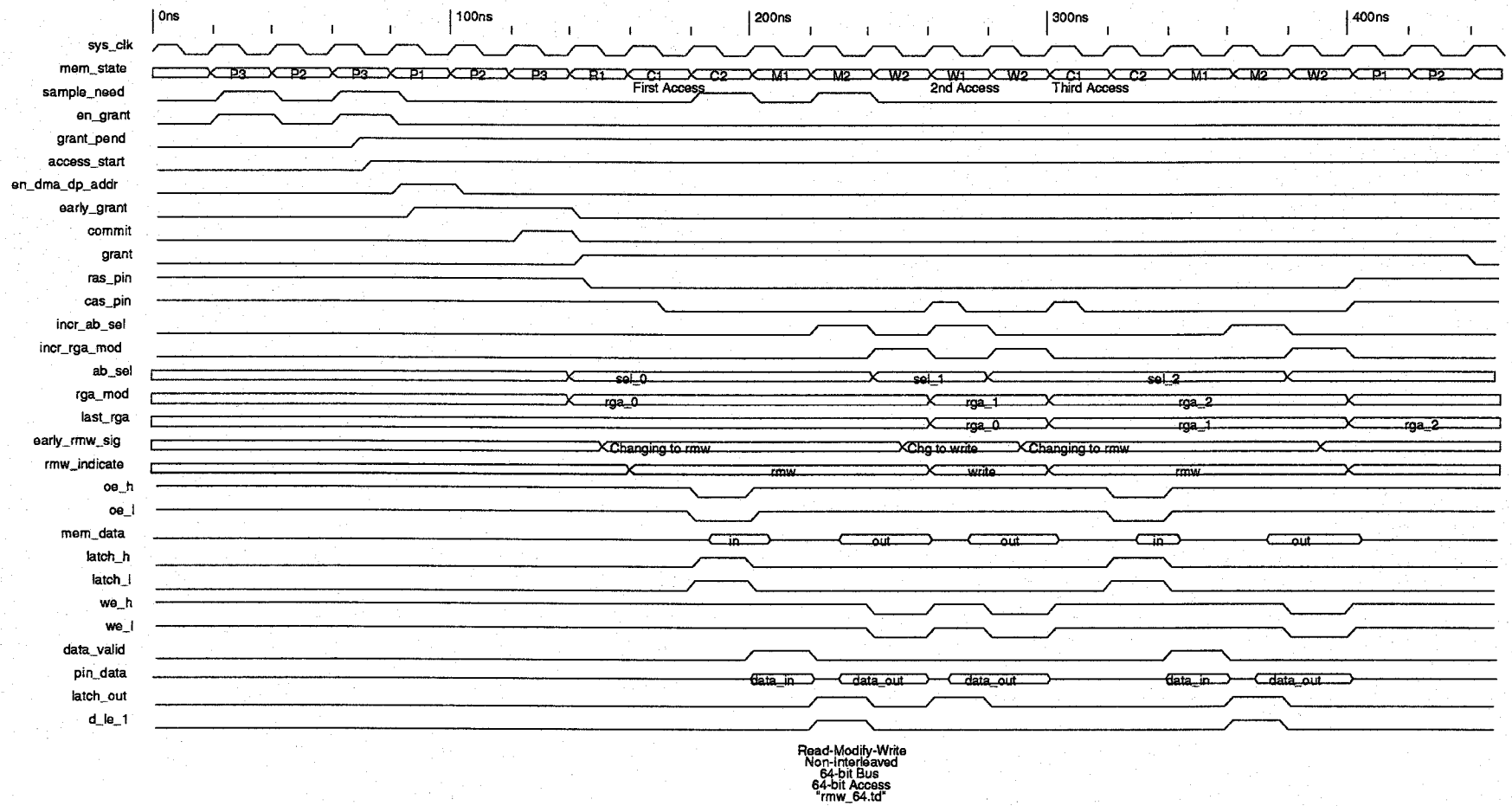
64-bit Memory RMW Access



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Circuit Size Estimates

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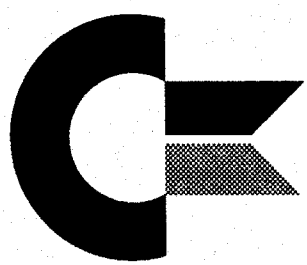

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Design Methodology

- **0.6 micron - 3 level metal CMOS - 3.3 Volt process**
- **Structured custom design technique**
  - **Datapaths (highly regular structures): full custom**
  - **Control logic: Synthesized via AutoLogic (M models)**
- **Design Tools**
  - **Schematic Capture: Design Architect (Mentor)**
  - **Simulation (Behavioral): Lsim (Mentor)**
  - **Simulation (Switch): Lsim (Mentor)**
  - **Simulation (Circuit): Hspice (MetaSoftware)**
  - **Synthesis: AutoLogic (Mentor)**
  - **Layout: Cadence**
  - **Place and Route (Standard Cells): AutoCells (Mentor)**
  - **Chip Assembly (Block place and route): SCII (Silver-Lisco)**
  - **Netlisting Tools: Commodore Proprietary**

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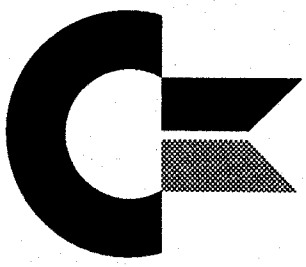

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Status...

- **Schematics for many major blocks have been captured**
- **M language, synthesizable, behavioral models have been written for much of the functionality of the chip set.**
- **Some simulation has been started, much remains to be done.**

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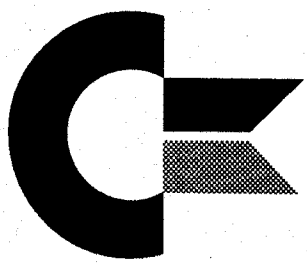

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Future?

- **Rambus? version**
- **Single Chip version**

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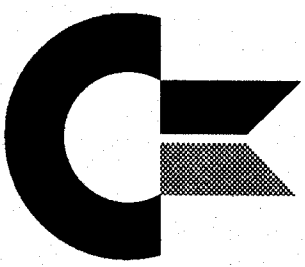

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What do WE want?

- License to produce an implementation of PA-RISC
- Architecture validation suite
  - Instruction test sequences
  - Emulators
- Software generation tools
  - C and C++ Compilers
  - Assembler - we need to modify for our enhancements
  - Other tools...
- IEEE Floating Point Emulation Code
  - Study to determine if SFU instructions may be appropriate
- Access to higher end Operating Systems
  - UNIX
  - Windows/NT
- Link to higher end product line

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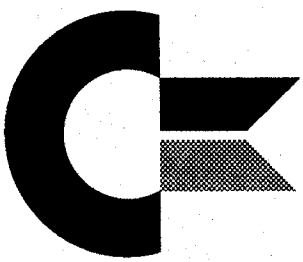

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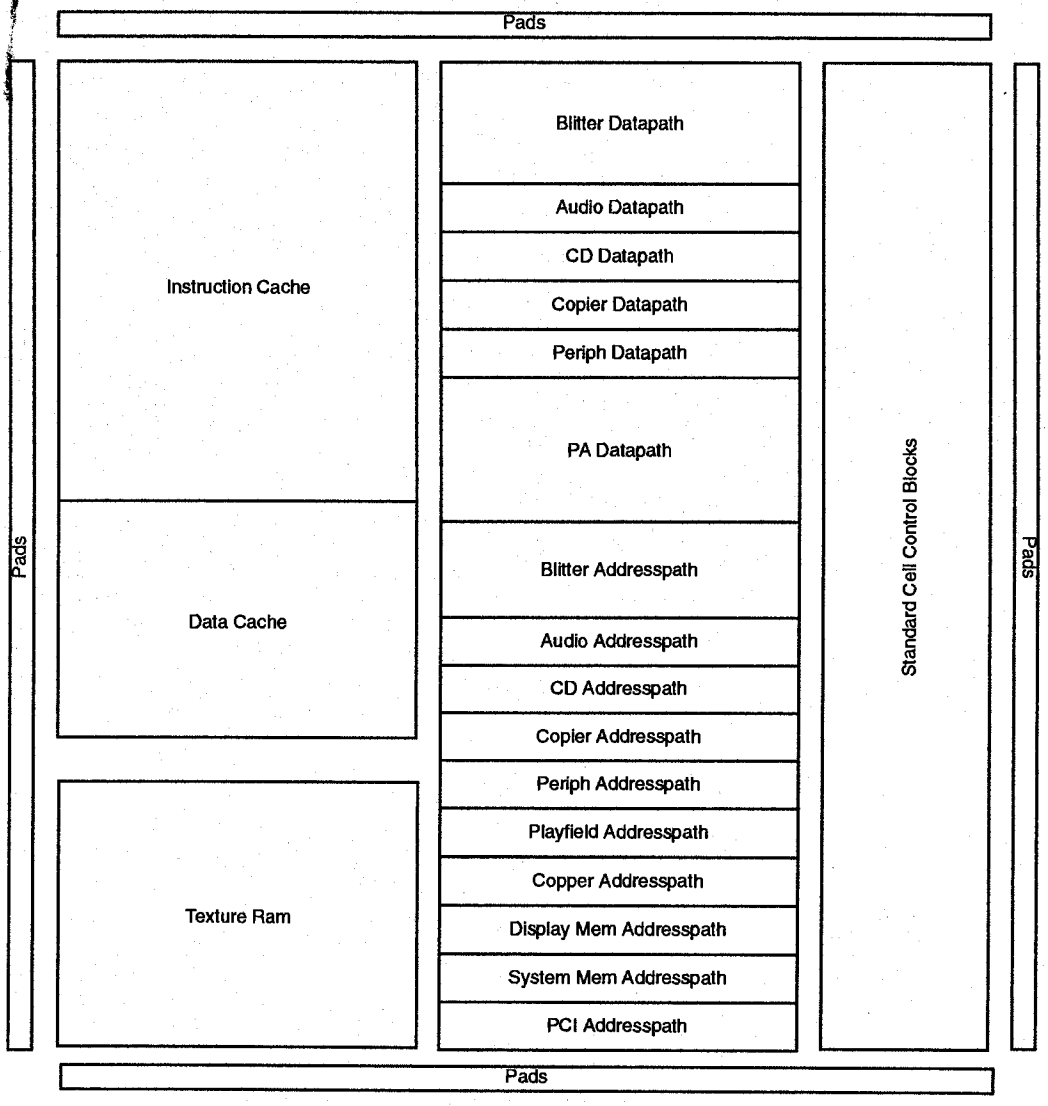
CPU Floorplan (First Cut)



- **0.6u Three-Layer Metal, 3V CMOS**
- **Estimate 9 x 9mm to 10mm x 10mm Die Size**

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